**CDAC Feb 2015**

**LAB 6**

Q2. 32 x 8 ROM

Name: Bhrigu Bhargava

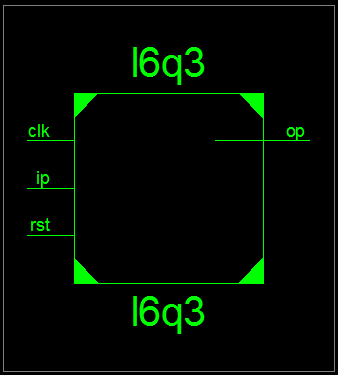
PRN: 150240133004

**32 x 8 ROM**

# Design Approach:

The 32x8 memory is designed using behavioural model. Here we generally design the 32x8 memory using the predefined functions like $readmemh and $fmonitor and sequential statements like if-else. Here we check for reset and clock edges. The values of input are stored in an external text file and then the same data is read and displayed as output.

**Block Diagram:**

****

**Fig 1:- Block Diagram**

**Source Code:**

module l6q2(output reg [7:0] op, input clk,oe,input [4:0] add);

reg [5:0] i=0;

integer id;

reg [7:0] val;

reg [7:0] memrom [31:0];

initial

begin

id=$fopen("memory.txt");

for(i=0;i<32;i=i+1)

begin

$fdisplay(id,"@%h %h",i,i);

end

$fclose(2);

$readmemh("memory.txt",memrom);

end

always @ (posedge clk)

begin

if(oe)

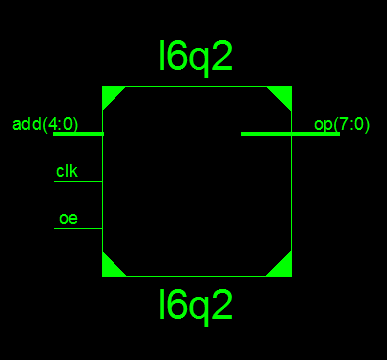
op <= memrom[add];

end

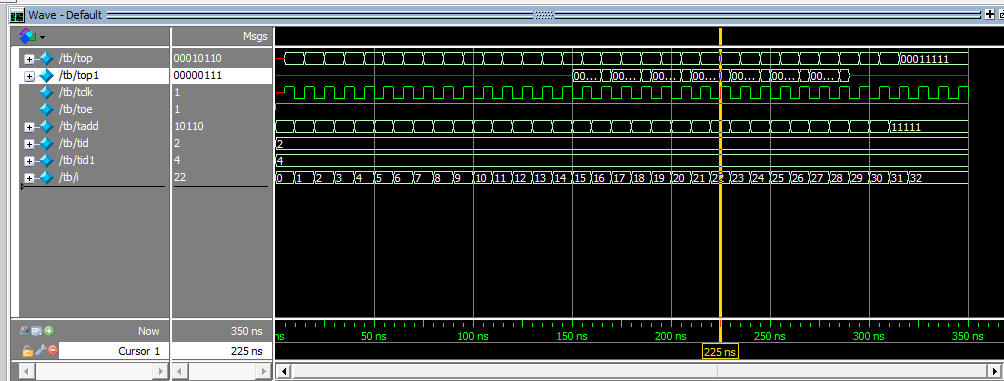
endmodule

**Synthesis:**

1. Block Diagram

****

1. Simulation Waveform Result

****

**Error:**

None

**Verified by:**

Dharamvir Chundawat (150240133007)